First Hit

Generate Collection Print

· L4: Entry 10 of 11

File: JPAB

Jun 18, 1986

PUB-NO: JP361131043A

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TITLE: INTER-TASK QUEUE CONTROLLING SYSTEM

PUBN-DATE: June 18, 1986

INVENTOR-INFORMATION:

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ASSIGNEE-INFORMATION:

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APPL-NO: JP59251756

APPL-DATE: November 30, 1984

INT-CL (IPC): G06F 9/46; G06F 11/34

ABSTRACT:

PURPOSE: To cope with a fault by only recording and erasing a relevant QUEUE entry in and from a check point file, by setting implementing order information indicating the implementing order of QUEUE entries in a relevant task in each QUEUE entry.

CONSTITUTION: When a system fault occurs, a CPU 41 first reads the content of a check point file 46 in an external storage device 44 into a <u>QUEUE entry pool</u> 60. Then the CPU 41 checks all <u>QUEUE entries in the pool</u> 60 and couples tasks by setting next entry <u>pointers</u> in the order of serial numbers at every task ID. Thereafter, the CPU 41 sets the location of a <u>QUEUE entry</u> 62 restored in the pool 60 in the first entry <u>pointer</u> of a control entry 61 in a queue control table 50 and the location of another <u>QUEUE entry</u> 63 in the final entry <u>pointer</u>. Furthermore, the CPU 41 sets the serial number 3 of the entry 63 in the serial number counter of the control entry 51.

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